

O I P E
MAR 13 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **TAKEMORI, Toshiyuki et al.**

Group Art Unit: **2814**

Serial No.: **09/660,439**

Examiner: **Steven H. RAO**

Filed: **September 12, 2000**

P.T.O. Confirmation No.: **6603**

For: **TRANSISTOR AND METHOD OF MANUFACTURING THE SAME**

AMENDMENT TRANSMITTAL

Commissioner for Patents
Washington, D.C. 20231

March 13, 2003

Sir:

Transmitted herewith is an Amendment in the above-identified application.
The fee has been calculated as shown below:

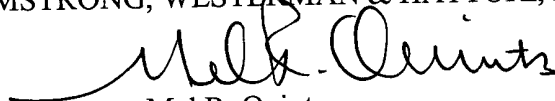
	CLAIMS AS AMENDED						
	Claims Remaining After Amendment	Highest Number Previously Paid For		Present Extra	Small Entity	Large Entity	Additional Fee
Total Claims	17	19	=	0	X \$9	X \$18	.00
Independent Claims	6	3	=	3	X \$42	X \$84	252.00
First Presentation of Multiple Dependent Claims					\$140	280	0.00
TOTAL FEES ENCLOSED:							252.00

XX Enclosed please find our check in the amount of \$252.00 for the additional claims fee in connection with this amendment.

XX The Commissioner is hereby authorized to charge payment for any additional fees associated with this communication or credit any overpayment to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



Mel R. Quintos
Attorney for Applicants
Reg. No. 31,898

MRQ:lrj

Atty. Docket No. **001155**
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PATENT TRADEMARK OFFICE

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PATENT & TRADEMARK

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re the Application of: **TAKEMORI, Toshiyuki et al.**

Group Art Unit: 2814

Serial No.: 09/660,439

Examiner: **Shrinivas (Steven) H. RAO**

Filed: **September 12, 2000**

P.T.O. Confirmation No.: 6603

For: **TRANSISTOR AND METHOD OF MANUFACTURING THE SAME**

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

March 13, 2003

Sir:

This is a Preliminary Amendment filed along with the Request for Continued Examination (RCE) filed March 13, 2003. Please amend the above-identified application as follows

IN THE CLAIMS:

Claims 1 and 11 have been amended as follows:

RECEIVED
MAR 18 2003
TECHNOLOGY CENTER 2800

1. (Twice Amended) A transistor comprising:

C1
a semiconductor substrate having a semiconductor layer, a drain layer of a first conductivity type provided on said semiconductor layer and a conductive region of a second conductivity type formed by diffusing an impurity of the second conductivity type from a surface of said drain layer;